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April 3, 2002

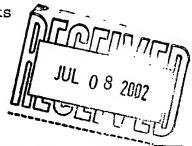
To: Commissioner of Patents and Trademarks

Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572

20 McIntosh Drive

Poughkeepsie, N.Y. 12603



Subject:

Serial No. 10/060,483 01/30/02

Yen-Ming Chen et al.

NOVEL METHOD TO IMPROVE BUMP RELIABILITY FOR FLIP CHIP DEVICE

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 10, 2002.

Stephen B. Ackerman, Reg.# 37763

Signature/Date

TSMC-01-413

- U.S. Patent 5,543,253 to Park et al., "Photomask for T-Gate Formation and Process for Fabricating the Same, " discusses a dual damascene like Photo process for a T-gate.
- U.S. Patent 6,042,996 to Lin et al., "Method of Fabricating a Dual Damascene Structure, " discusses a dual damascene process.

The following four U.S. Patents disclose Bump and UBM processes:

- U.S. Patent 6,232,212 to Degani et al., "Flip Chip 1) Bump Bonding."
- U.S. Patent 6,153,503 to Lin et al., "Continuous 2) Process for Producing Solder Bumps on Electrodes of Semiconductor Chips."
- U.S. Patent 6,130,141 to Degani et al., "Flip Chip 3) Metallization."
- 4) U.S. Patent 6,118,180 to Loo et al., "Semiconductor Die Metal Layout for Flip Chip Packaging."

Sincerely,

phen B. Ackerman,

Reg. No. 37761

citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.